FIG.1A

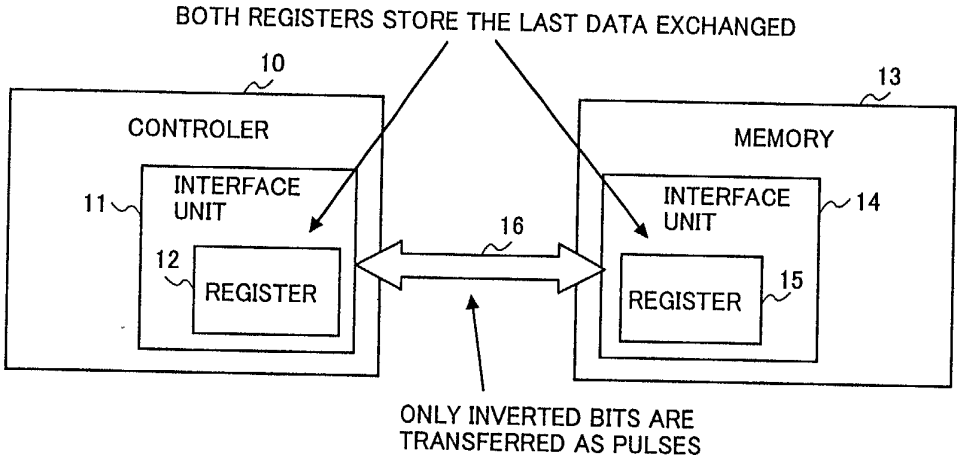

BOTH REGISTERS STORE THE LAST DATA EXCHANGED
10
CONTROLER
11
INTERFACE UNIT
12
REGISTER
16
13
MEMORY
INTERFACE UNIT
14
REGISTER
15
ONLY INVERTED BITS ARE TRANSFERRED AS PULSES

FIG.1B

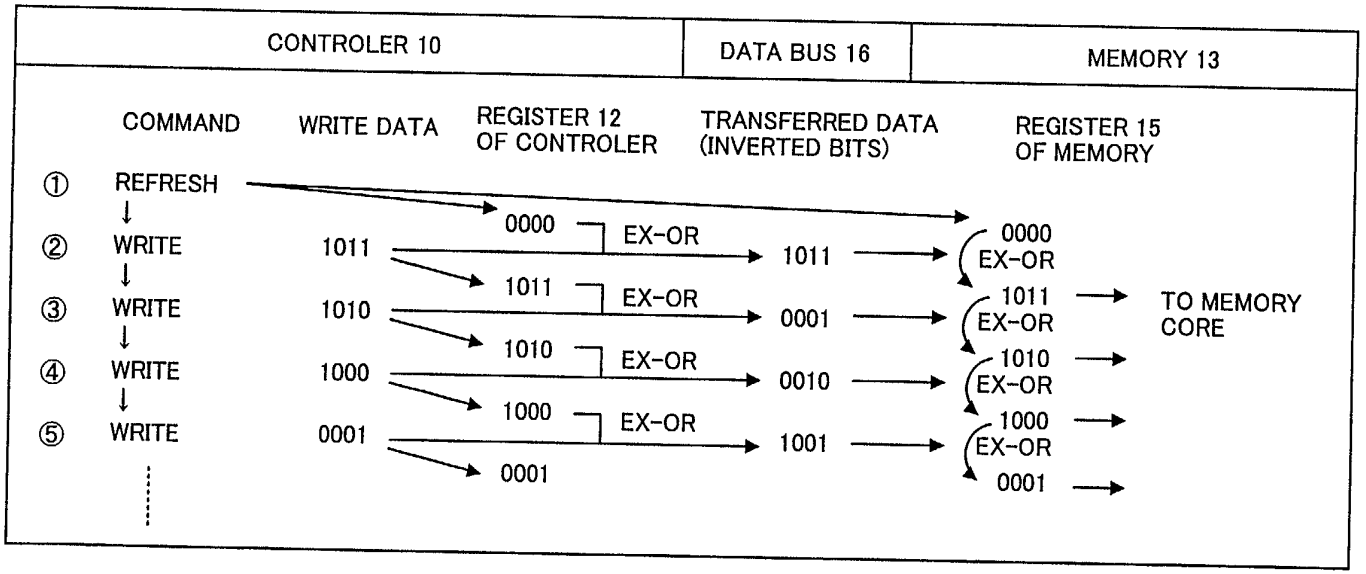

CONTROLER 10
DATA BUS 16
MEMORY 13
COMMAND
WRITE DATA
REGISTER 12 OF CONTROLER
TRANSFERRED DATA (INVERTED BITS)
REGISTER 15 OF MEMORY
① REFRESH
② WRITE
③ WRITE
④ WRITE
⑤ WRITE
1011
1010
1000
0001
0000
EX-OR
TO MEMORY CORE

FIG.2

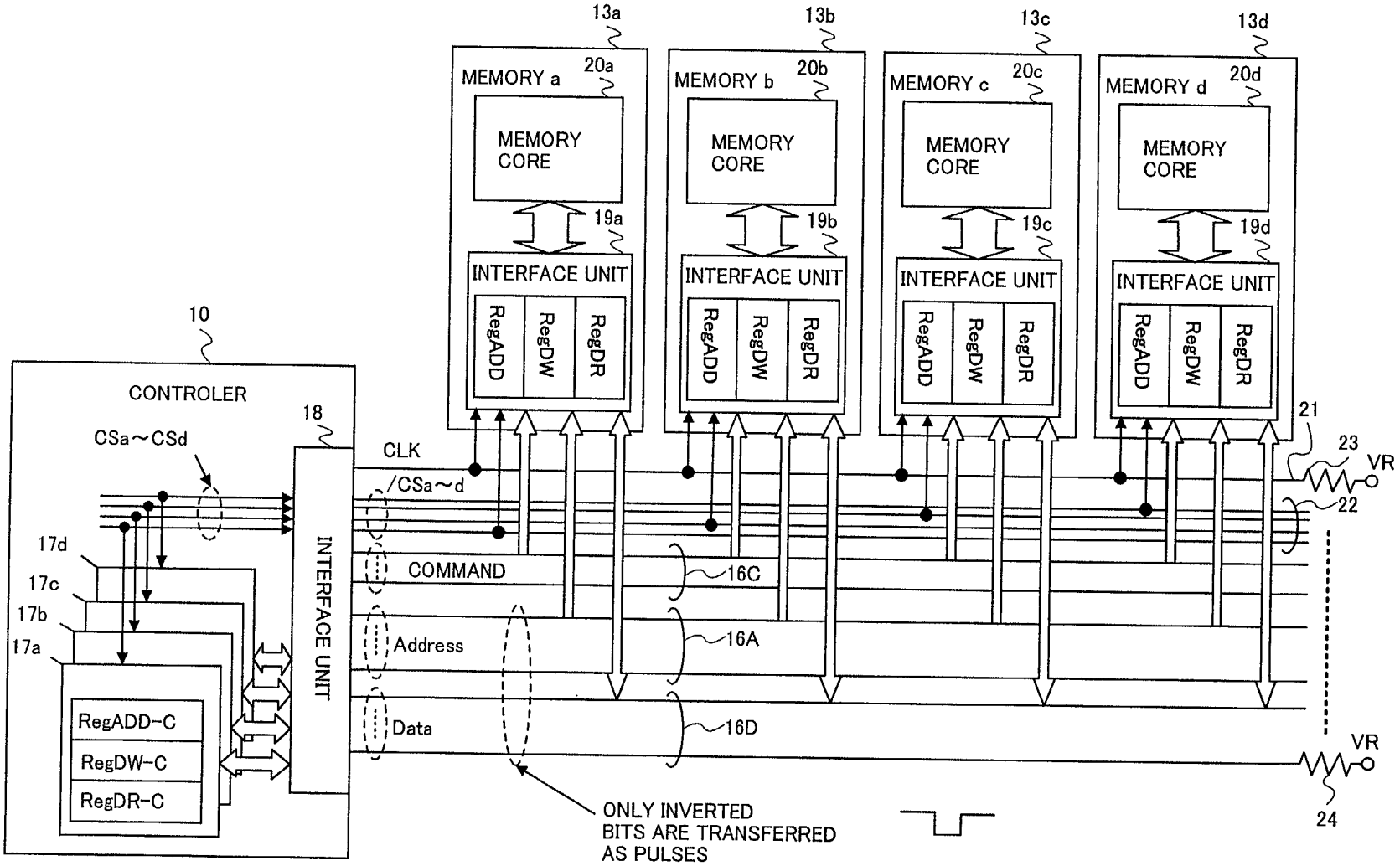

13a
13b
13c
13d
MEMORY a
20a
MEMORY b
20b
MEMORY c
20c
MEMORY d
20d
MEMORY CORE
19a
19b
19c
19d
INTERFACE UNIT
RegADD
RegDW
RegDR
10
CONTROLER
18
CSa~CSd
CLK
/CSa~d
COMMAND
Address
Data
16C
16A
16D
17d
17c
17b
17a
RegADD-C
RegDW-C
RegDR-C
INTERFACE UNIT
21
23
VR
22
VR
24
ONLY INVERTED
BITS ARE TRANSFERRED
AS PULSES

FIG.3

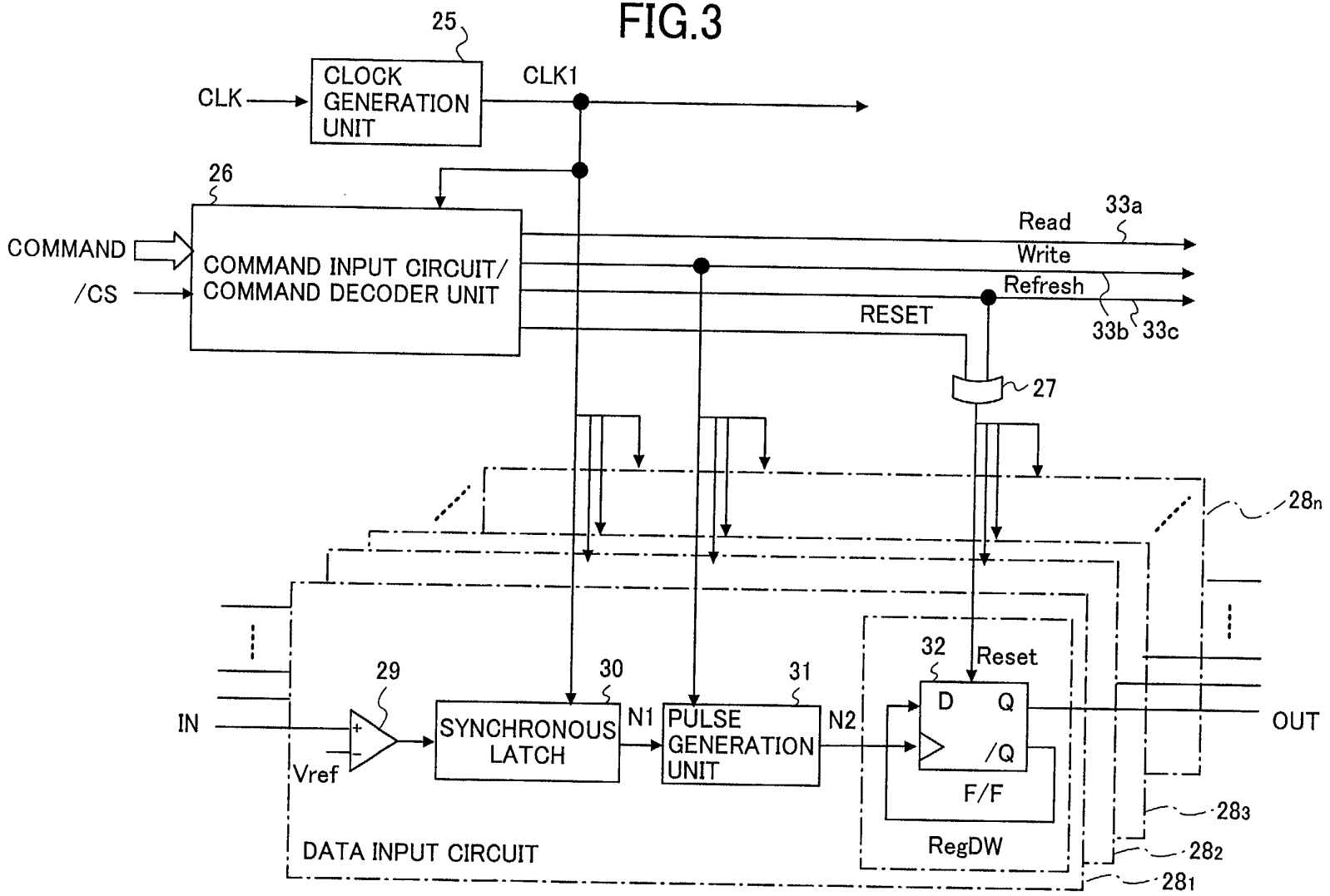

25
CLOCK GENERATION UNIT
CLK
CLK1
26
COMMAND
/CS
COMMAND INPUT CIRCUIT/ COMMAND DECODER UNIT
Read
Write
Refresh
RESET
33a
33b
33c
27
28n
29
30
31
32
Reset
IN
Vref
SYNCHRONOUS LATCH
N1
PULSE GENERATION UNIT
N2
D
Q
/Q
F/F
OUT
DATA INPUT CIRCUIT
RegDW
283
282
281

FIG. 4

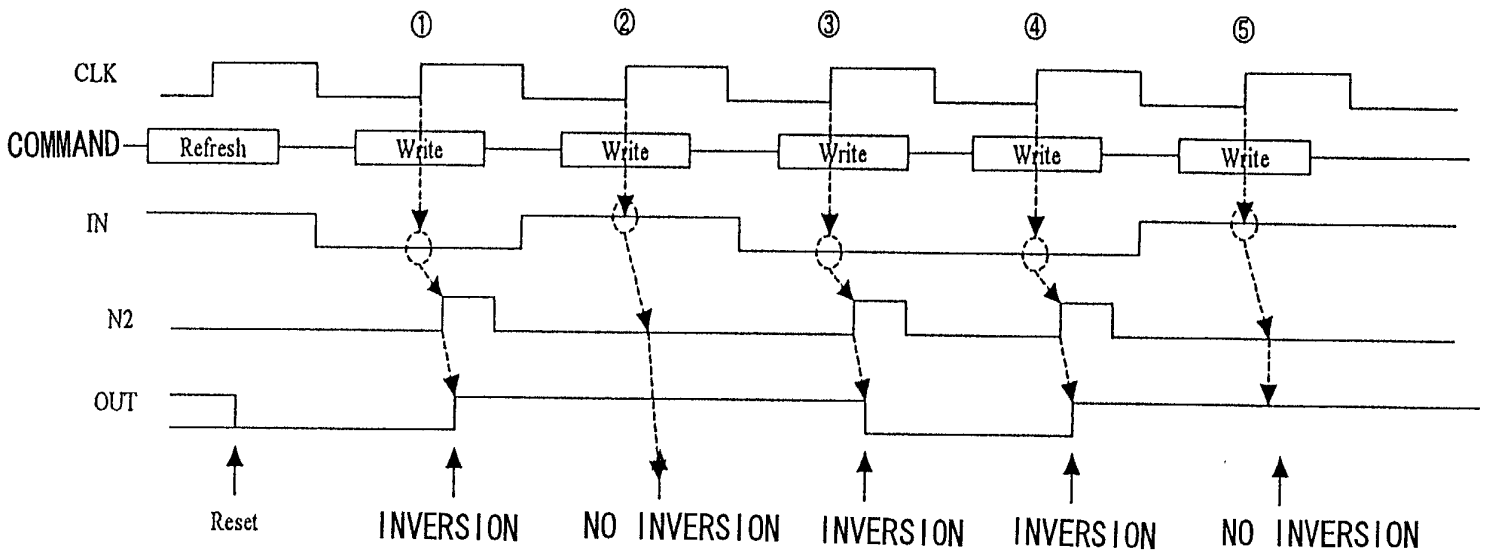

①
②
③
④
⑤
CLK
COMMAND
Refresh
Write
Write
Write
Write
Write
IN
N2
OUT
Reset
INVERSION
NO INVERSION
INVERSION
INVERSION
NO INVERSION

FIG.5

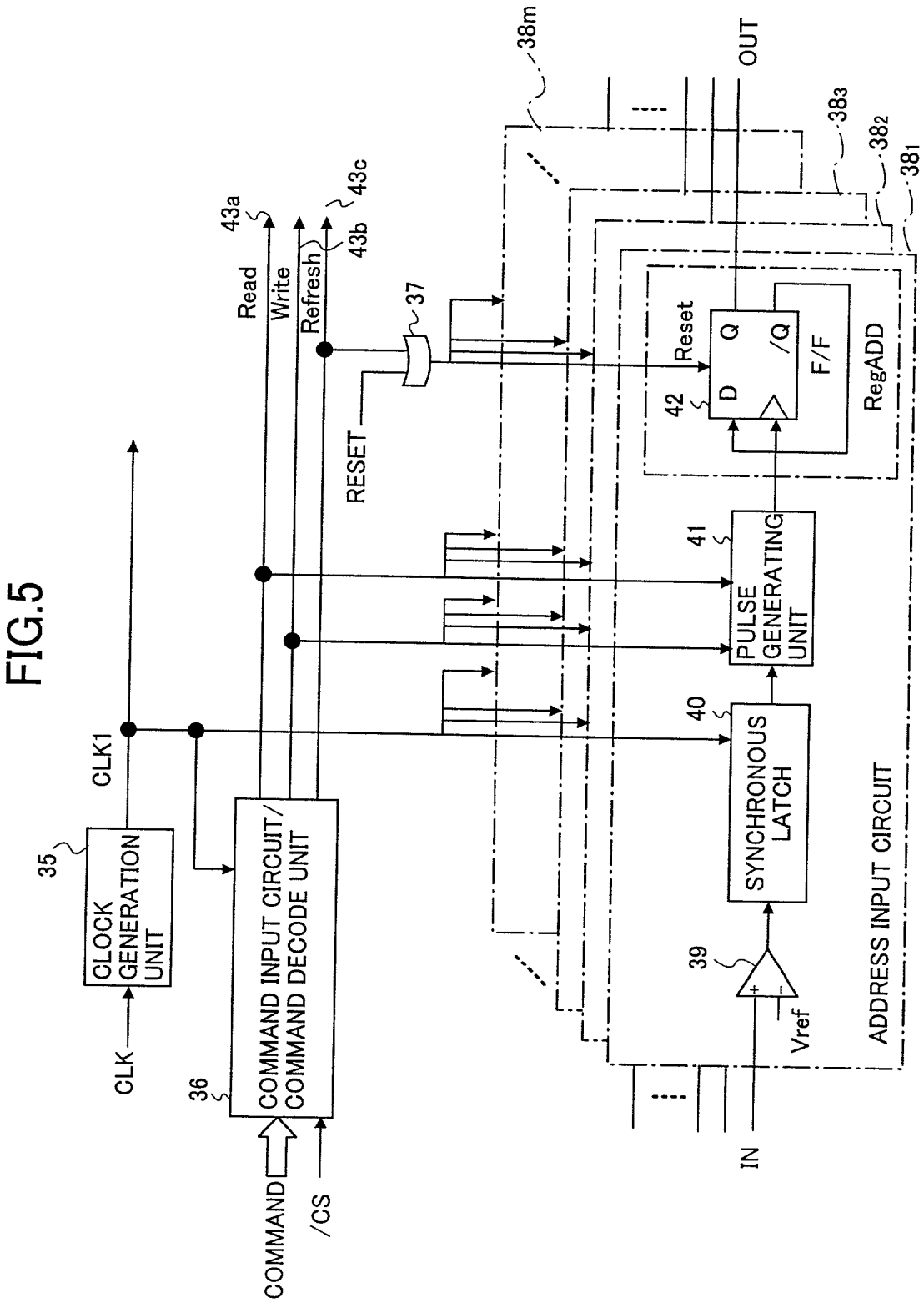

CLOCK GENERATION UNIT
35
CLK
CLK1
COMMAND INPUT CIRCUIT/ COMMAND DECODE UNIT
36
COMMAND
/CS
Read
Write
Refresh
43a
43b
43c
RESET
37
SYNCHRONOUS LATCH
40
PULSE GENERATING UNIT
41
Reset
D
Q
/Q
F/F
42
RegADD
39
Vref
IN
OUT
38m
38₃
38₂
38₁
ADDRESS INPUT CIRCUIT

FIG.6

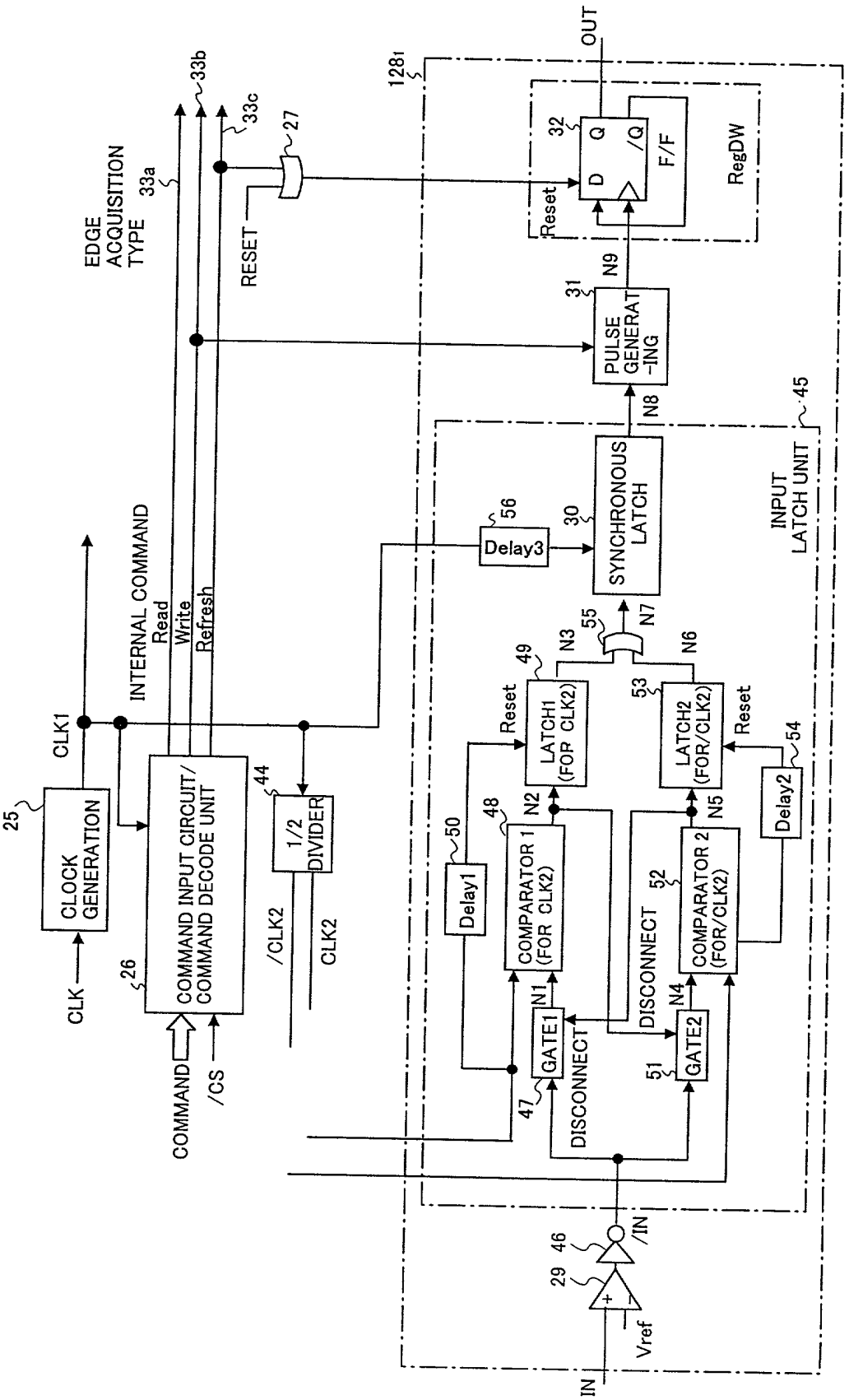

CLOCK GENERATION
25
CLK
CLK1
COMMAND INPUT CIRCUIT/ COMMAND DECODE UNIT
26
COMMAND
/CS
INTERNAL COMMAND
Read
Write
Refresh
1/2 DIVIDER
44
/CLK2
CLK2
EDGE ACQUISITION TYPE
33a
33b
33c
27
RESET
128i
OUT
32
D
Q
/Q
F/F
Reset
RegDW
31
PULSE GENERAT -ING
N9
N8
45
INPUT LATCH UNIT
Delay3
56
30
SYNCHRONOUS LATCH
N7
55
N3
N6
49
LATCH1 (FOR CLK2)
53
LATCH2 (FOR/CLK2)
Reset
54
Delay2
Delay1
50
48
COMPARATOR 1 (FOR CLK2)
N2
N5
52
COMPARATOR 2 (FOR/CLK2)
DISCONNECT
N1
N4
GATE1
GATE2
51
47
DISCONNECT
46
/IN
29
Vref
IN

FIG.7

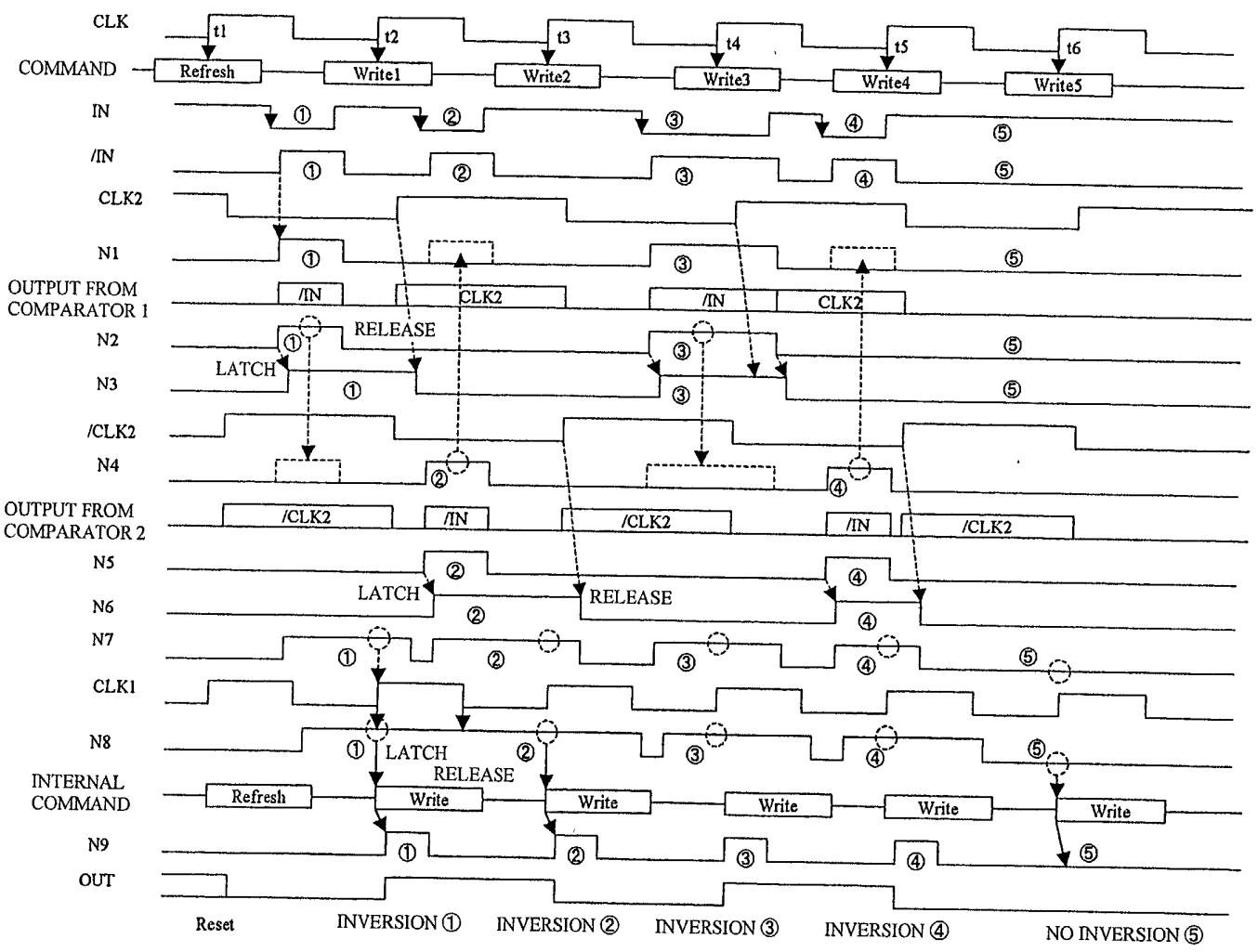

CLK
COMMAND
IN
/IN
CLK2
N1
OUTPUT FROM COMPARATOR 1
N2
N3
/CLK2
N4
OUTPUT FROM COMPARATOR 2
N5
N6
N7
CLK1
N8
INTERNAL COMMAND
N9
OUT
t1
t2
t3
t4
t5
t6
Refresh
Write1
Write2
Write3
Write4
Write5
/IN
CLK2
RELEASE
LATCH
/CLK2
/IN
/CLK2
/IN
/CLK2
LATCH
RELEASE
LATCH
RELEASE
Refresh
Write
Write
Write
Write
Write
Reset
INVERSION ①
INVERSION ②
INVERSION ③
INVERSION ④
NO INVERSION ⑤

FIG.8

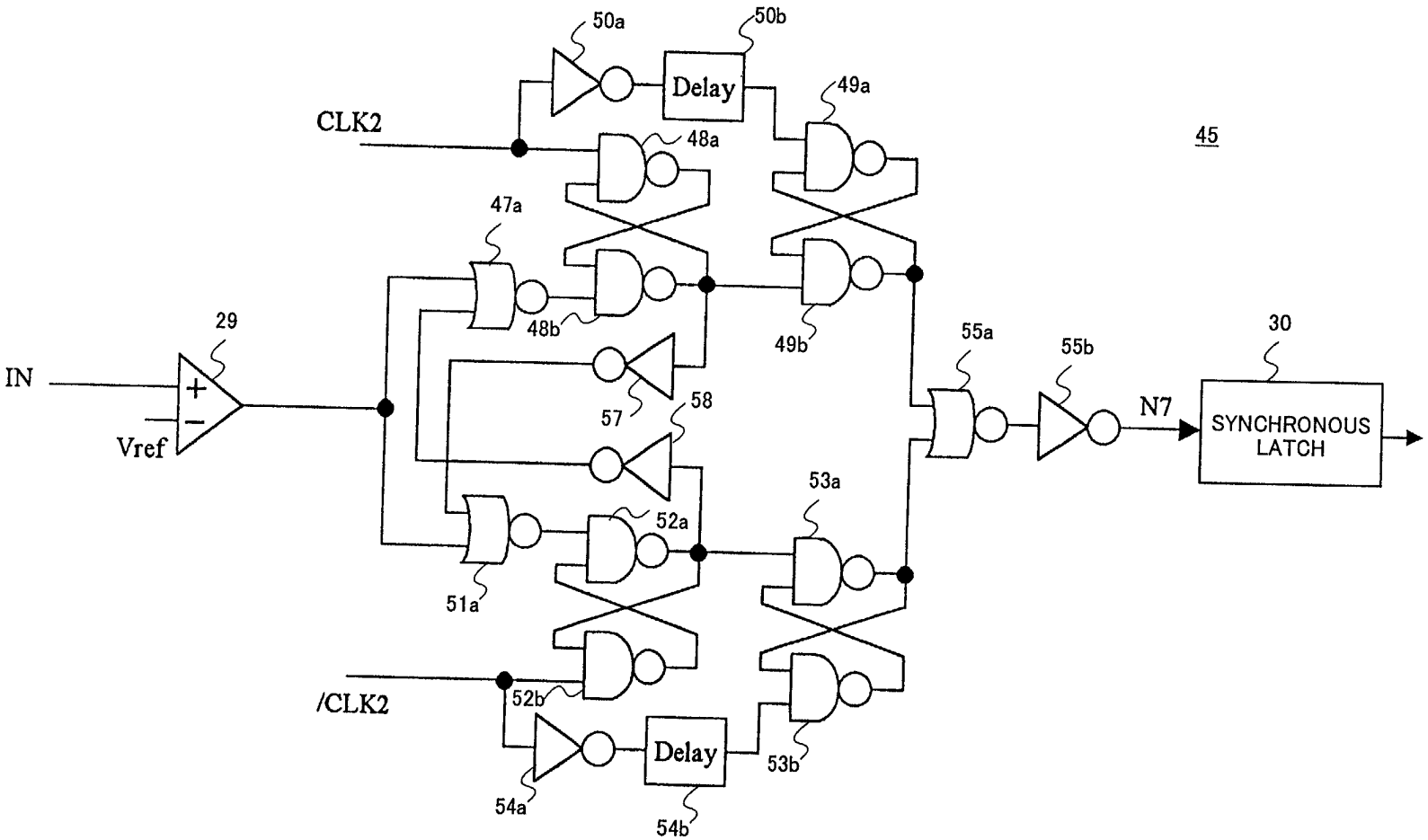


FIG.9

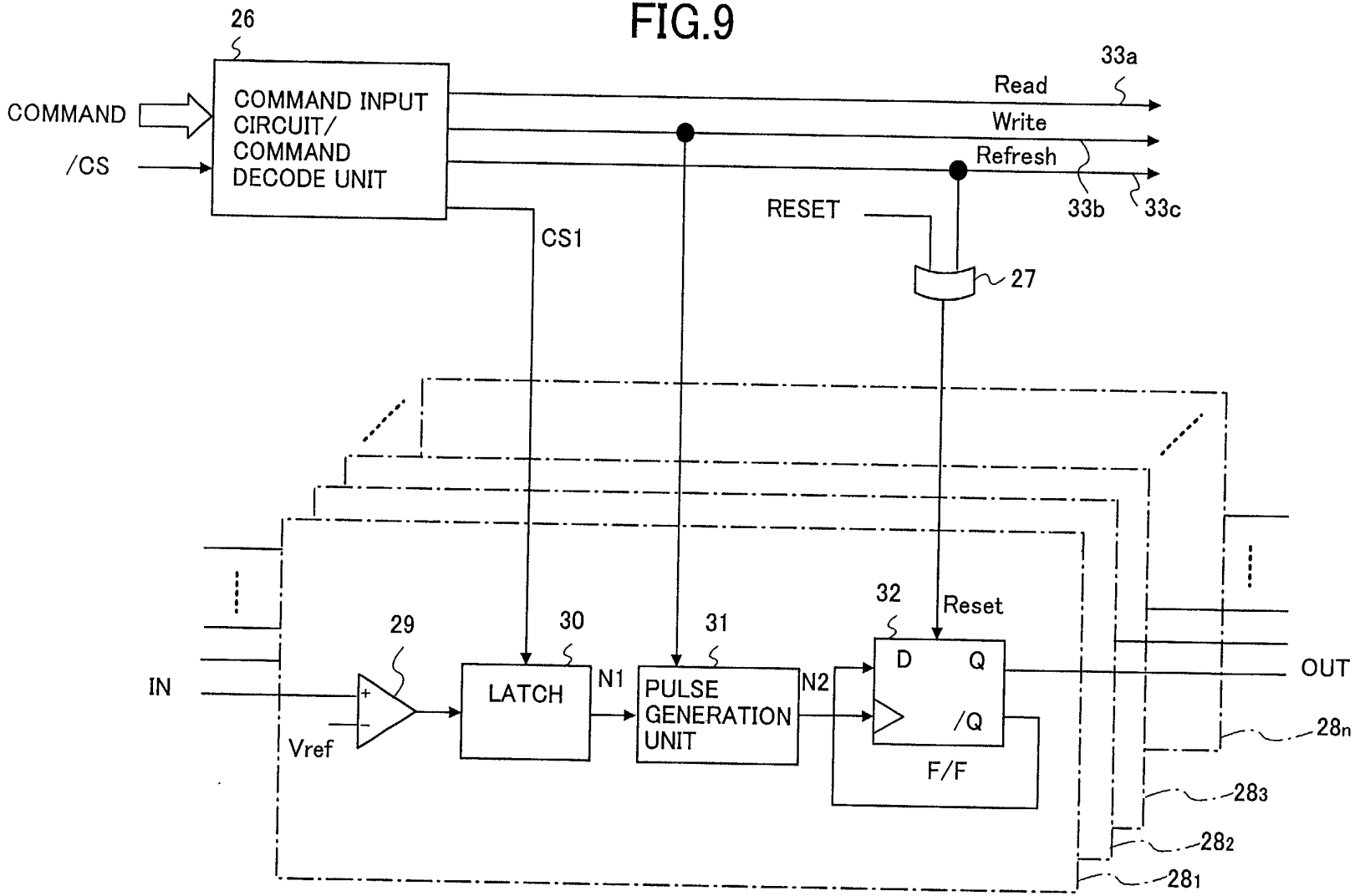


FIG. 10

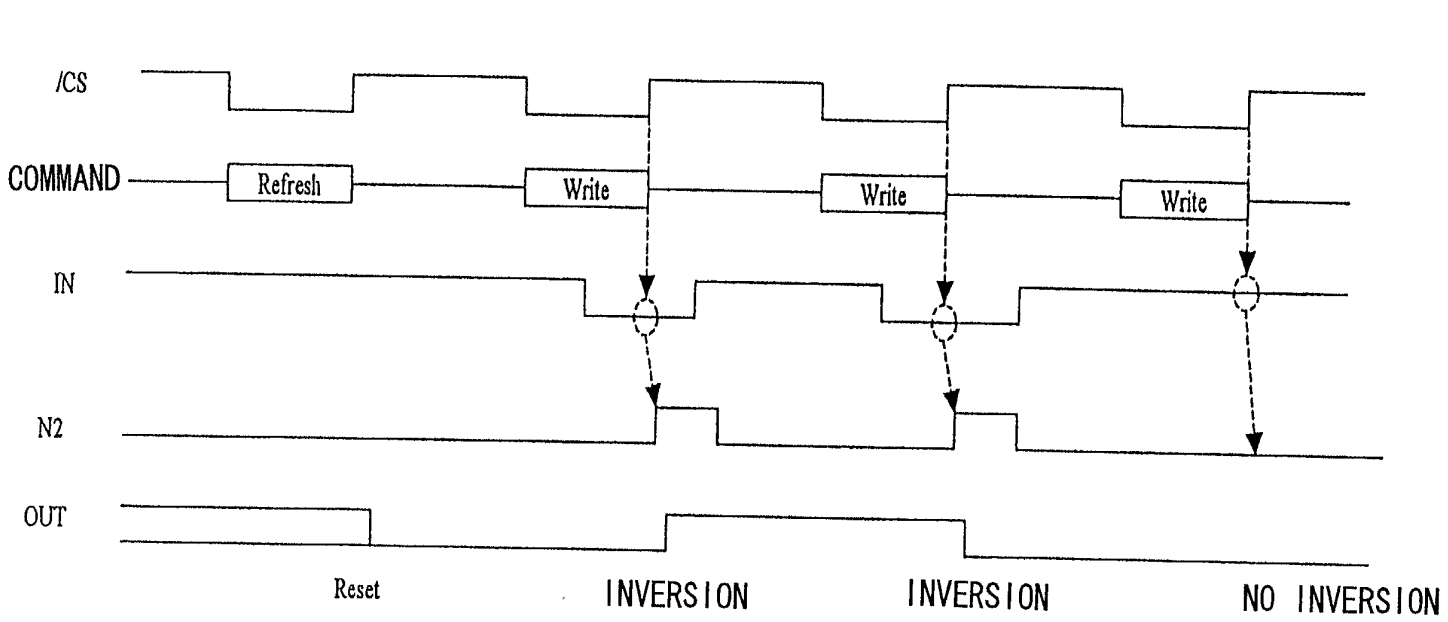


FIG.11

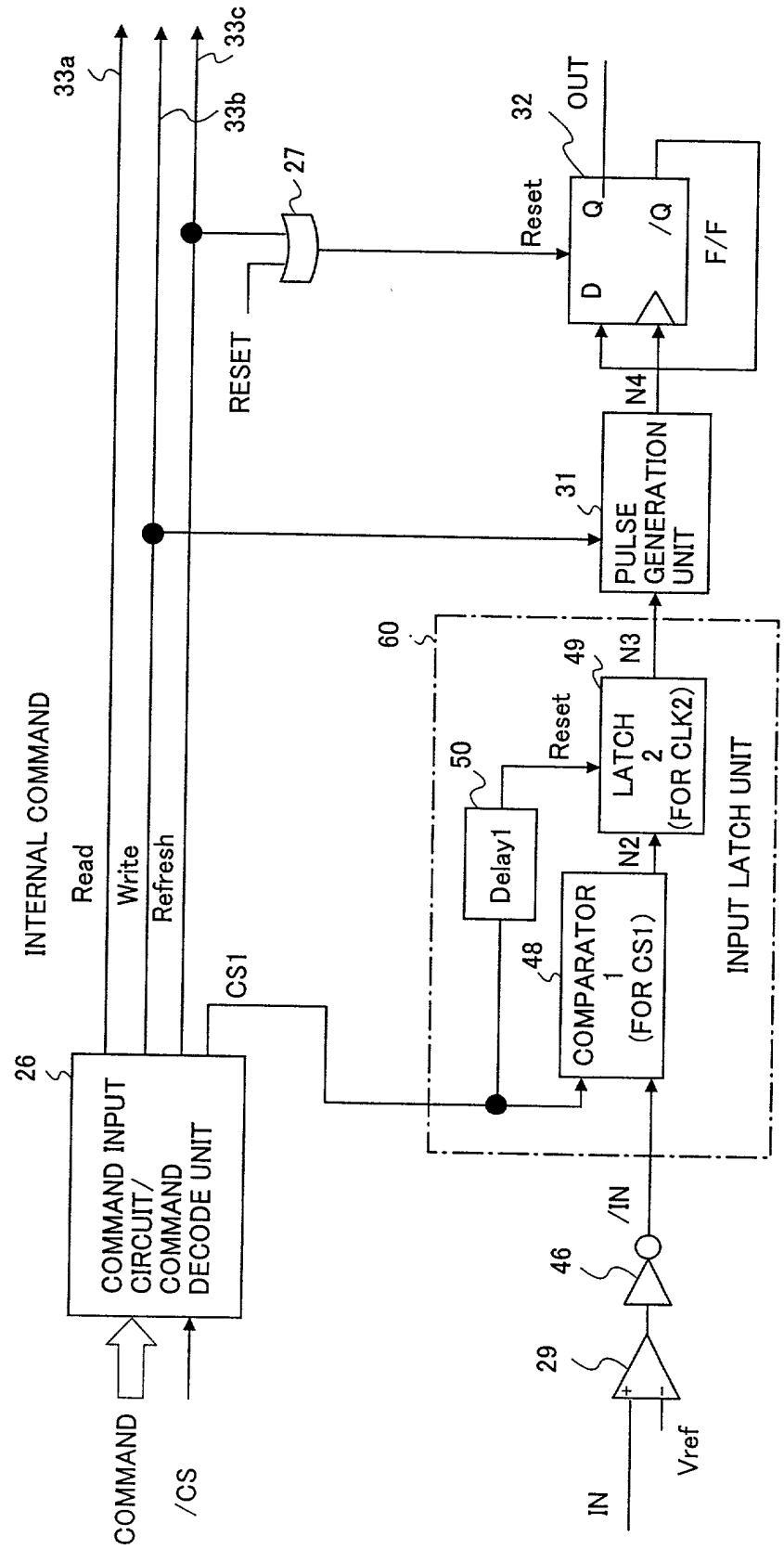

COMMAND
/CS
COMMAND INPUT CIRCUIT/ COMMAND DECODE UNIT
26
INTERNAL COMMAND
Read
Write
Refresh
CS1
33a
33b
33c
RESET
27
Reset
D
Q
/Q
F/F
32
OUT
PULSE GENERATION UNIT
31
N4
60
INPUT LATCH UNIT
Delay1
50
Reset
LATCH 2 (FOR CLK2)
49
N3
COMPARATOR 1 (FOR CS1)
48
N2
/IN
46
29
IN
Vref

FIG. 12

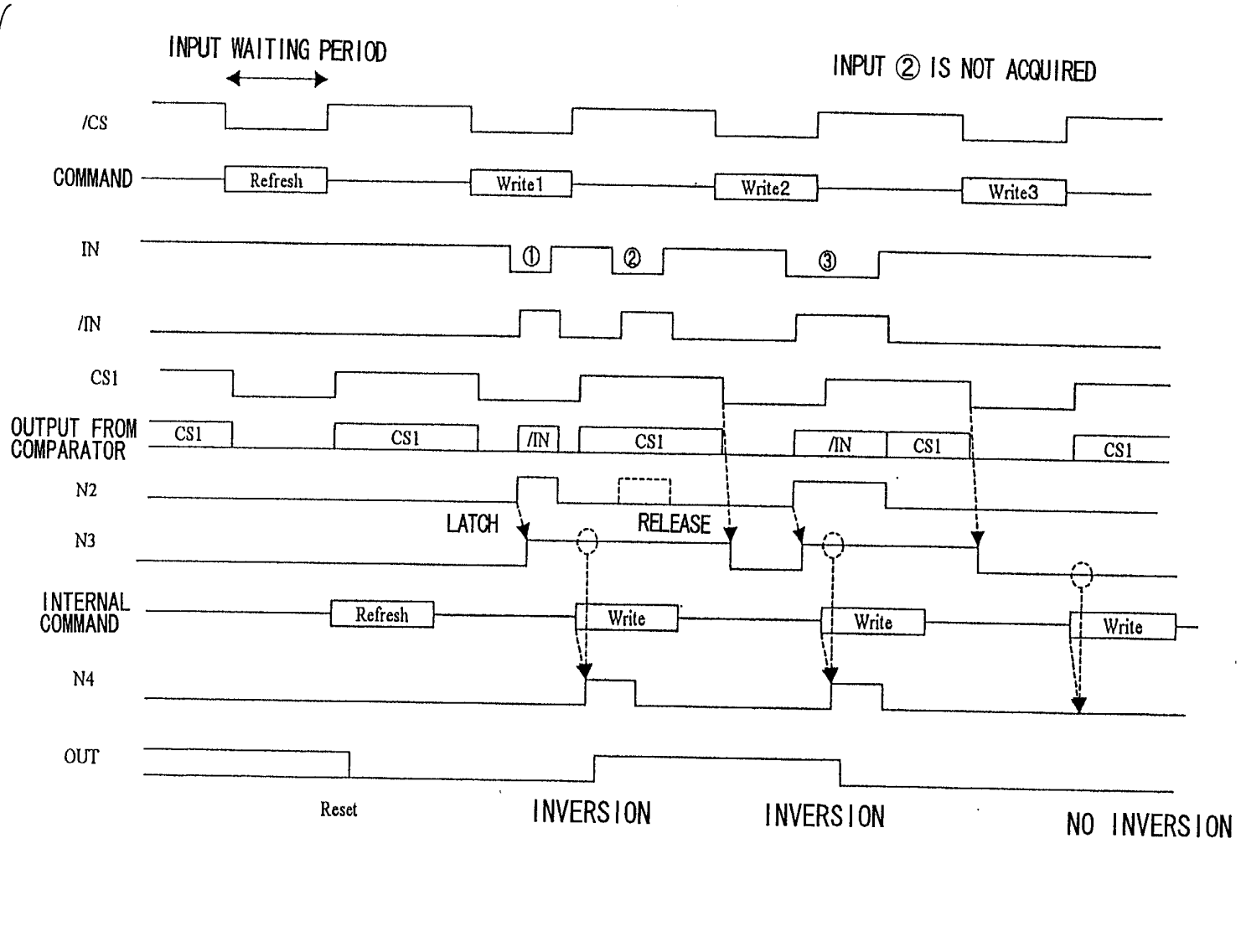

INPUT WAITING PERIOD
INPUT ② IS NOT ACQUIRED
/CS
COMMAND
Refresh
Write1
Write2
Write3
IN
①
②
③
/IN
CS1
OUTPUT FROM COMPARATOR
CS1
CS1
/IN
CS1
/IN
CS1
CS1
N2
LATCH
RELEASE
N3
INTERNAL COMMAND
Refresh
Write
Write
Write
N4
OUT
Reset
INVERSION
INVERSION
NO INVERSION

FIG.13

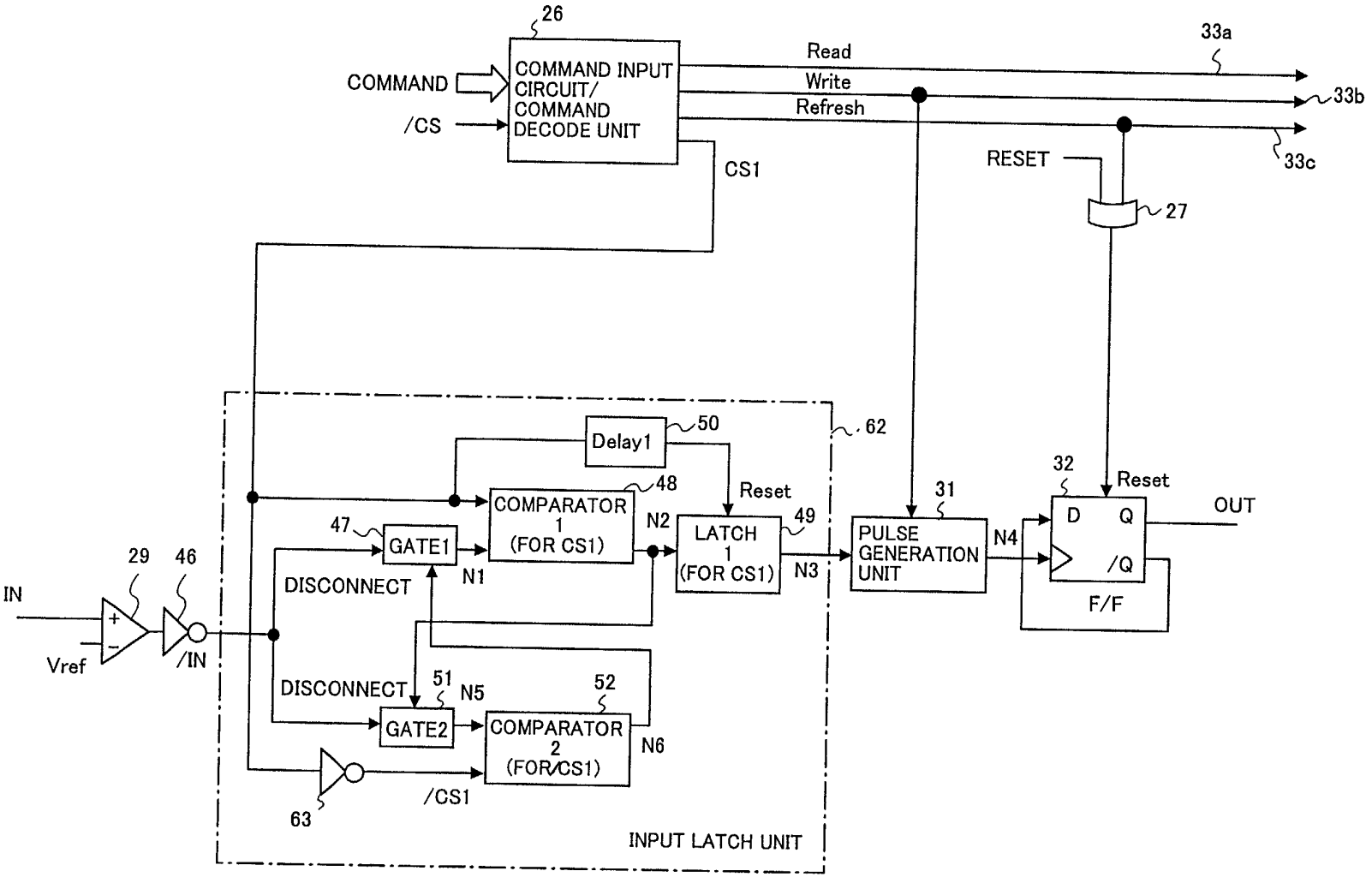

26
COMMAND
/CS
COMMAND INPUT CIRCUIT/ COMMAND DECODE UNIT
Read
Write
Refresh
33a
33b
33c
CS1
RESET
27
62
Delay1
50
Reset
48
COMPARATOR 1 (FOR CS1)
47
GATE1
N1
N2
LATCH 1 (FOR CS1)
49
N3
31
PULSE GENERATION UNIT
N4
32
Reset
D
Q
/Q
F/F
OUT
IN
29
46
Vref
/IN
DISCONNECT
DISCONNECT
51
N5
52
GATE2
COMPARATOR 2 (FOR/CS1)
N6
/CS1
63
INPUT LATCH UNIT

FIG.14

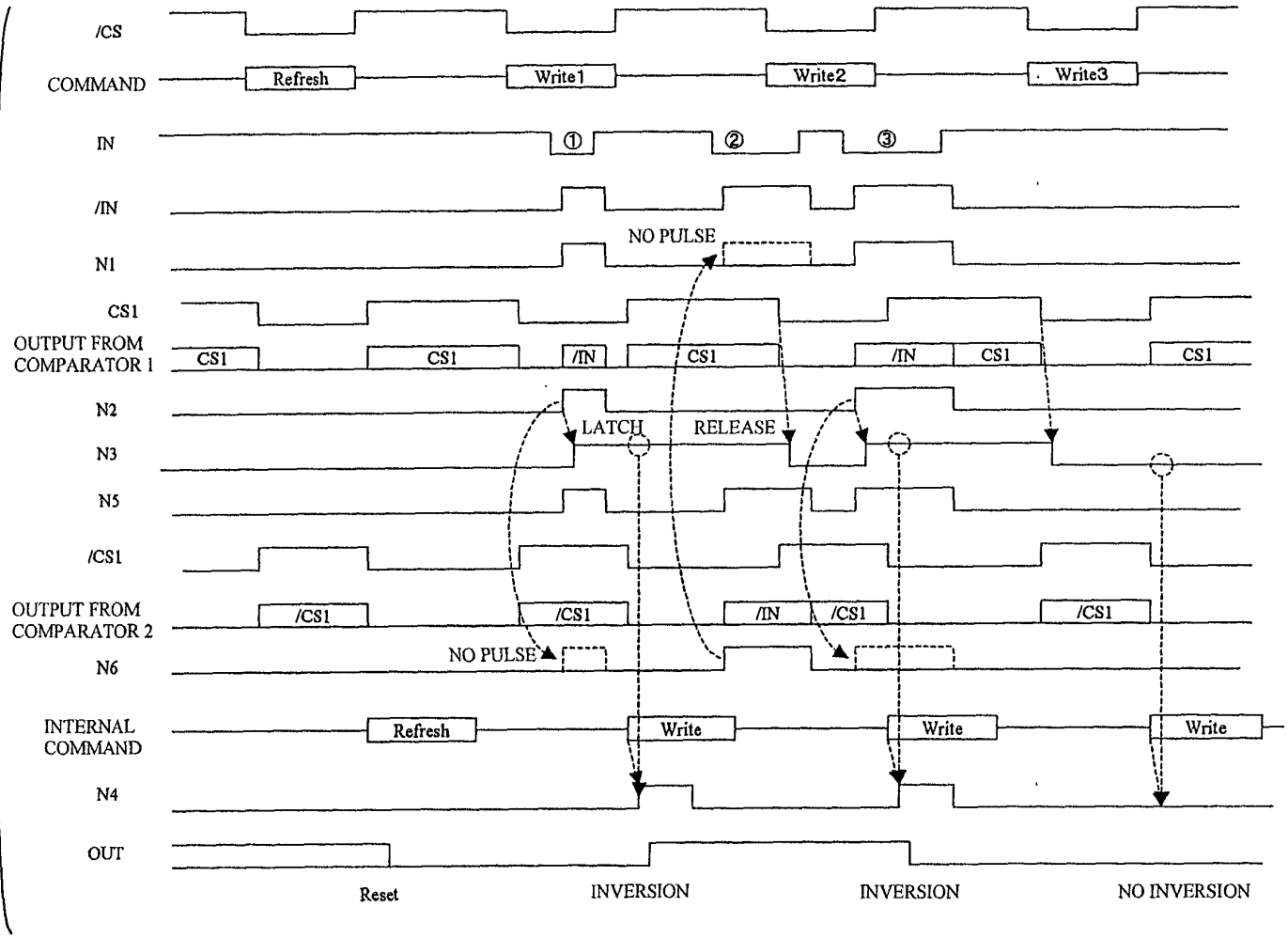

/CS
COMMAND
Refresh
Write1
Write2
Write3
IN
①
②
③
/IN
NO PULSE
N1
CS1
OUTPUT FROM COMPARATOR 1
CS1
CS1
/IN
CS1
/IN
CS1
CS1
N2
LATCH
RELEASE
N3
N5
/CS1
OUTPUT FROM COMPARATOR 2
/CS1
/CS1
/IN
/CS1
/CS1
NO PULSE
N6
INTERNAL COMMAND
Refresh
Write
Write
Write
N4
OUT
Reset
INVERSION
INVERSION
NO INVERSION

FIG.15

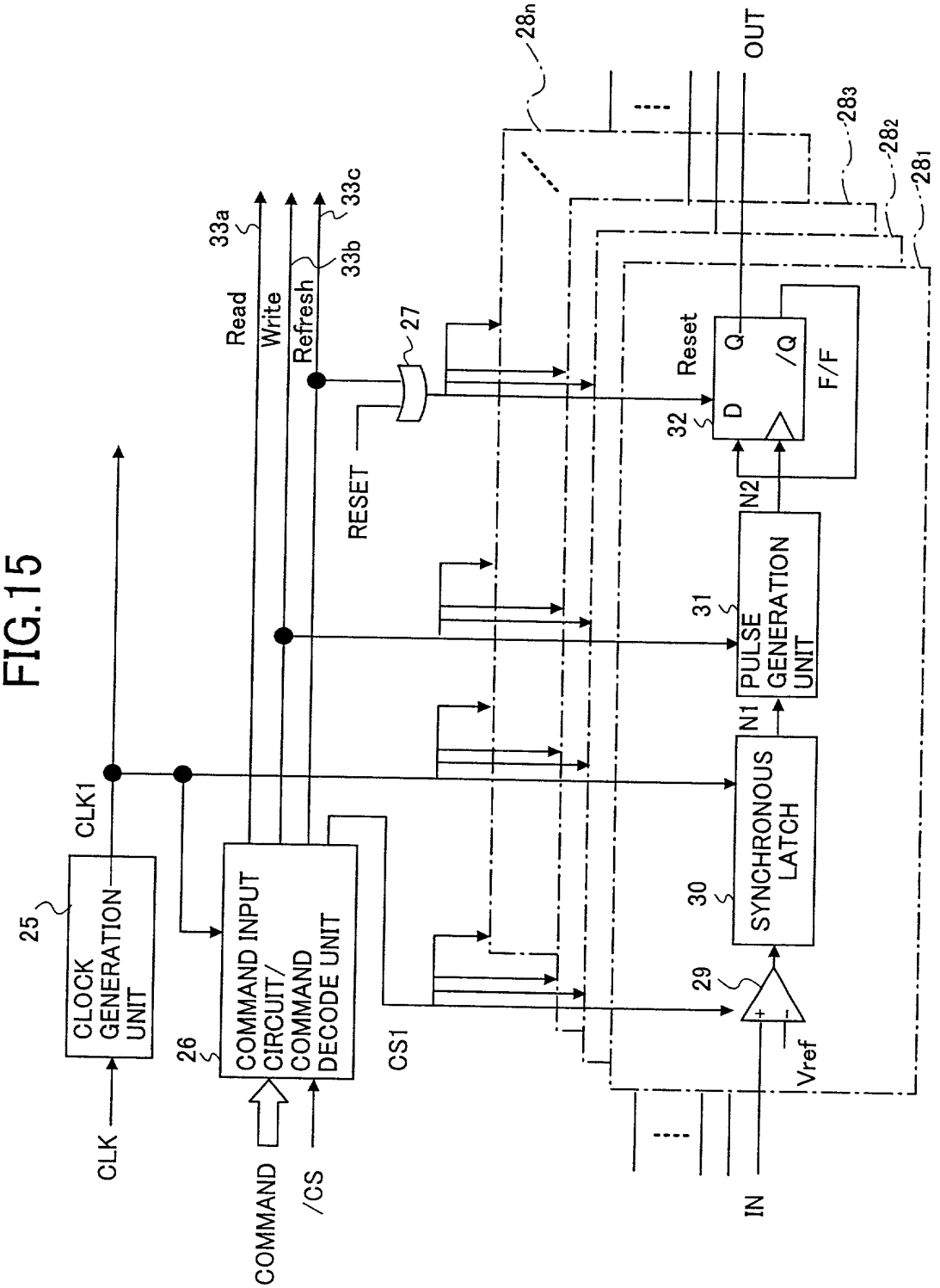


FIG. 16

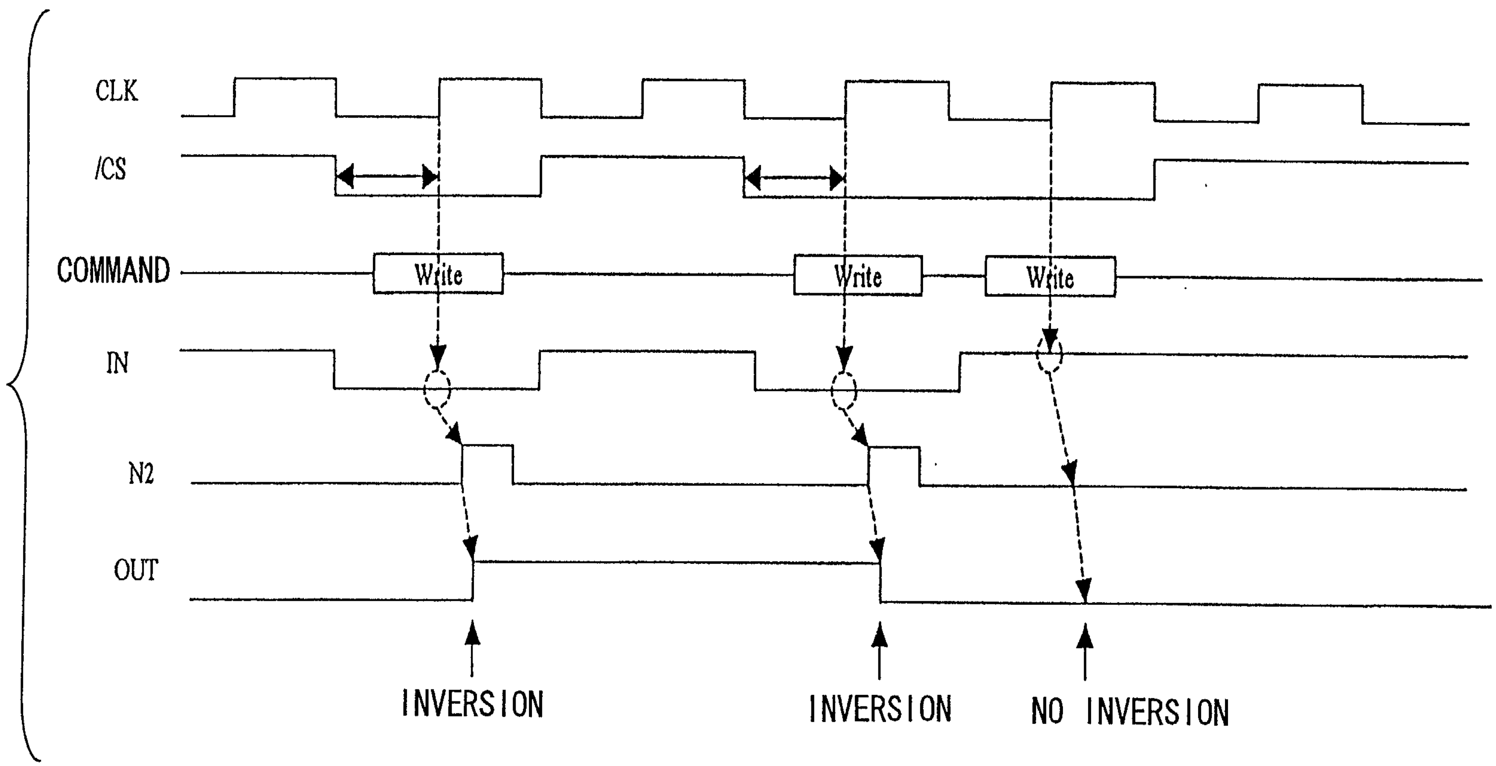

CLK
/CS
COMMAND
IN
N2
OUT
Write
Write
Write
INVERSION
INVERSION
NO INVERSION

FIG.17A

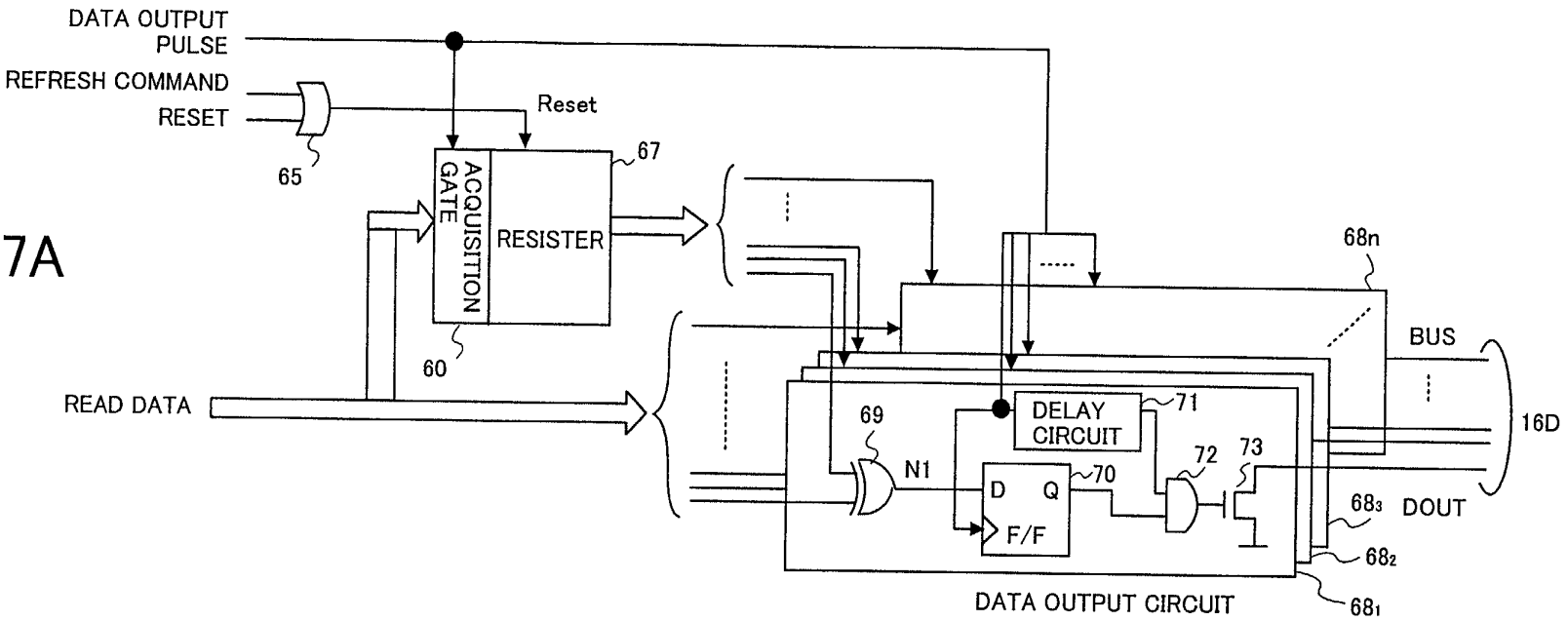


FIG.17B

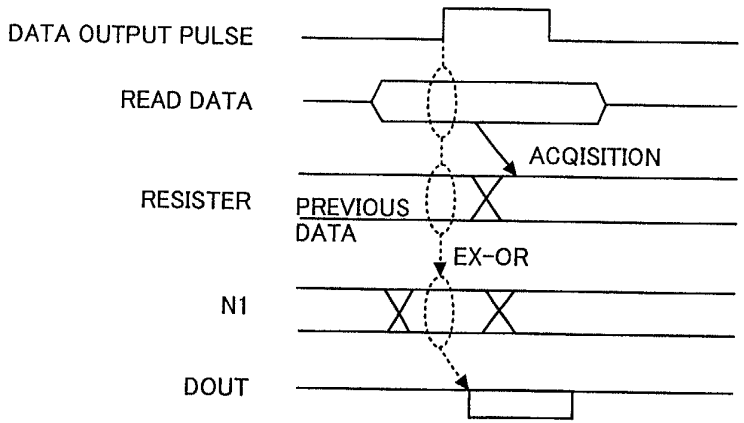


FIG.18

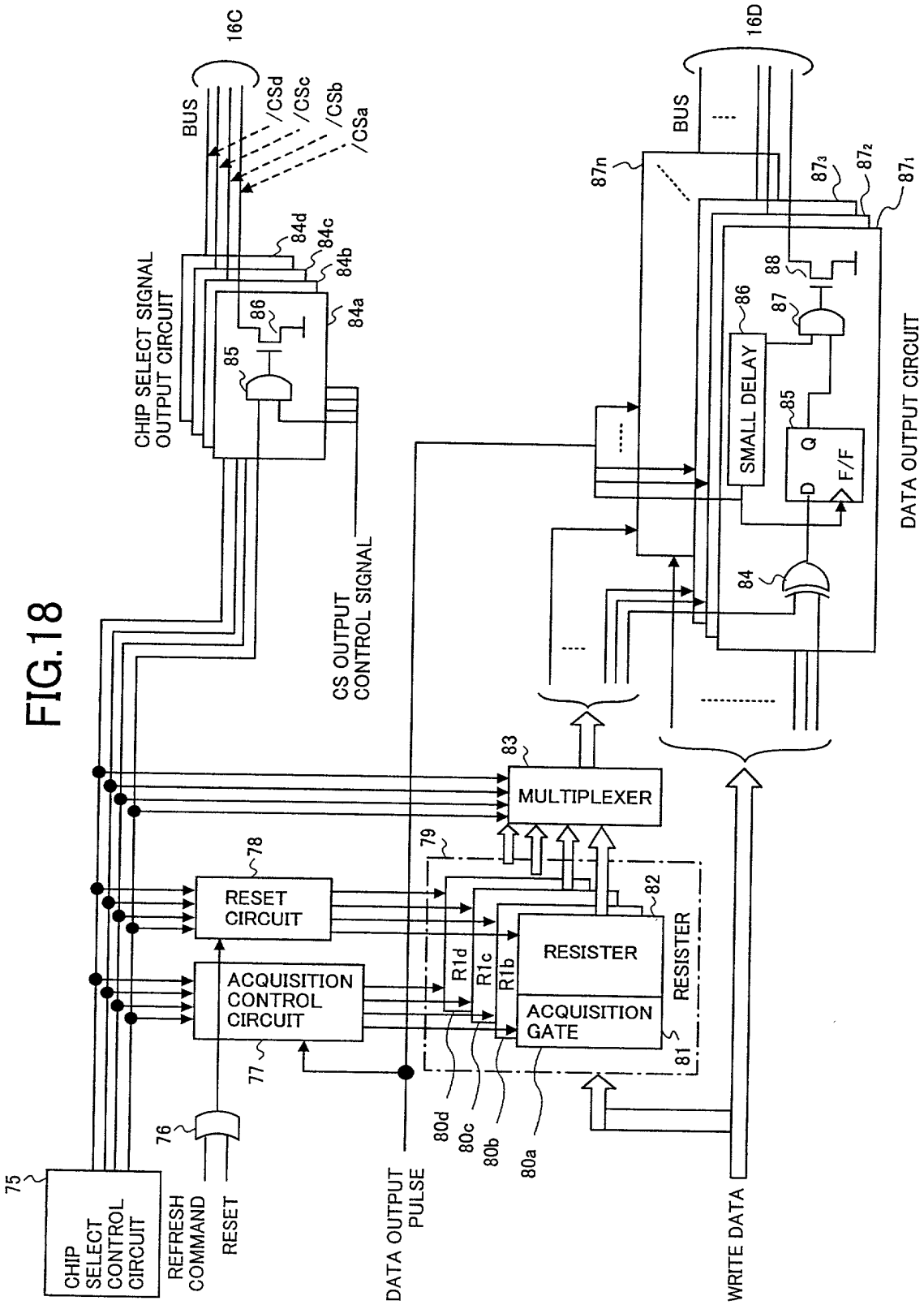


FIG.19

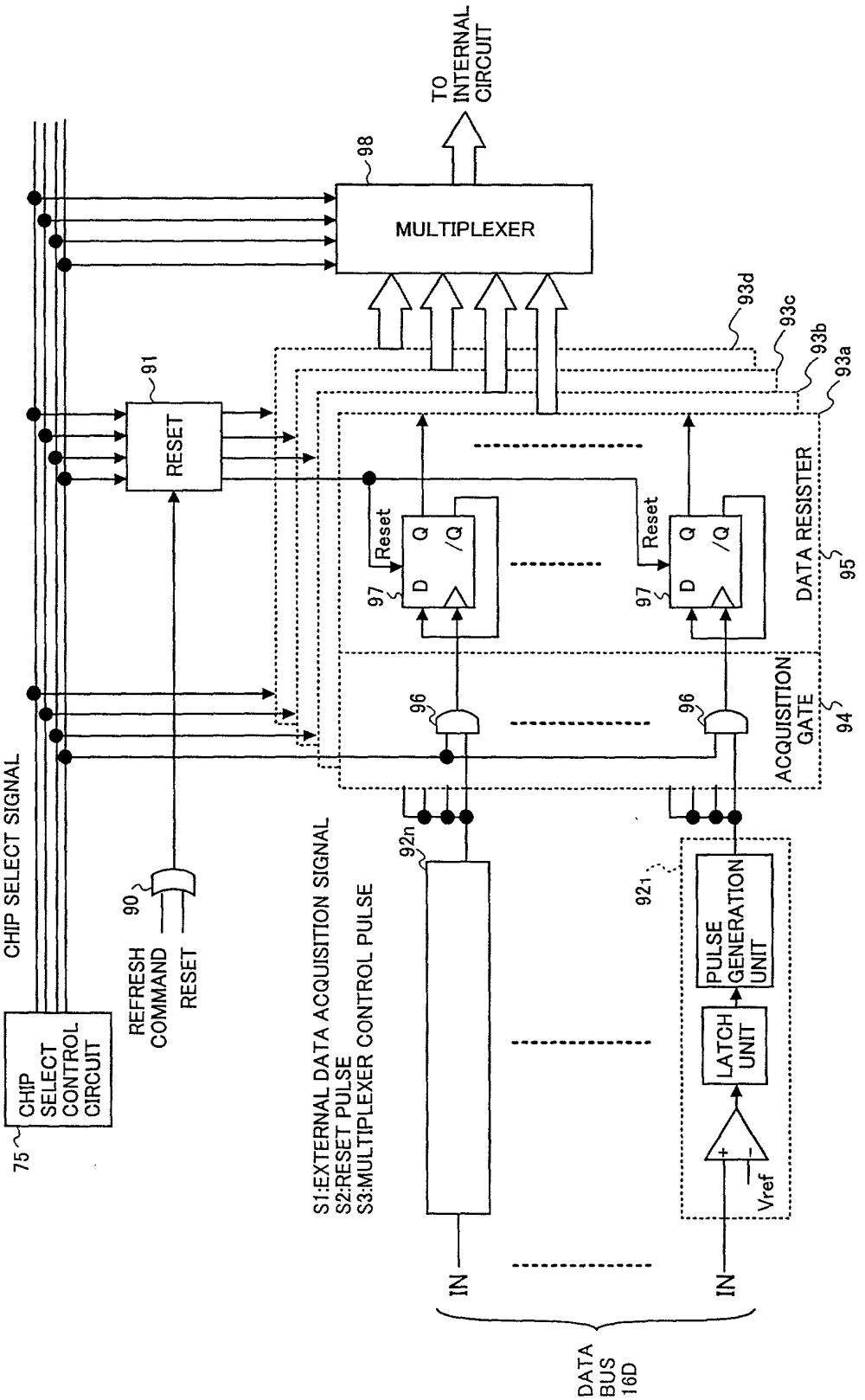

TO INTERNAL CIRCUIT
98
MULTIPLEXER
93d
93c
93b
93a
91
RESET
Reset
Q
/Q
D
97
DATA RESISTER
95
ACQUISITION GATE
94
96
CHIP SELECT SIGNAL
90
REFRESH COMMAND
RESET
S1:EXTERNAL DATA ACQUISITION SIGNAL
S2:RESET PULSE
S3:MULTIPLEXER CONTROL PULSE
92n
92₁
PULSE GENERATION UNIT
LATCH UNIT
Vref
IN
DATA BUS 16D
75
CHIP SELECT CONTROL CIRCUIT

FIG.20

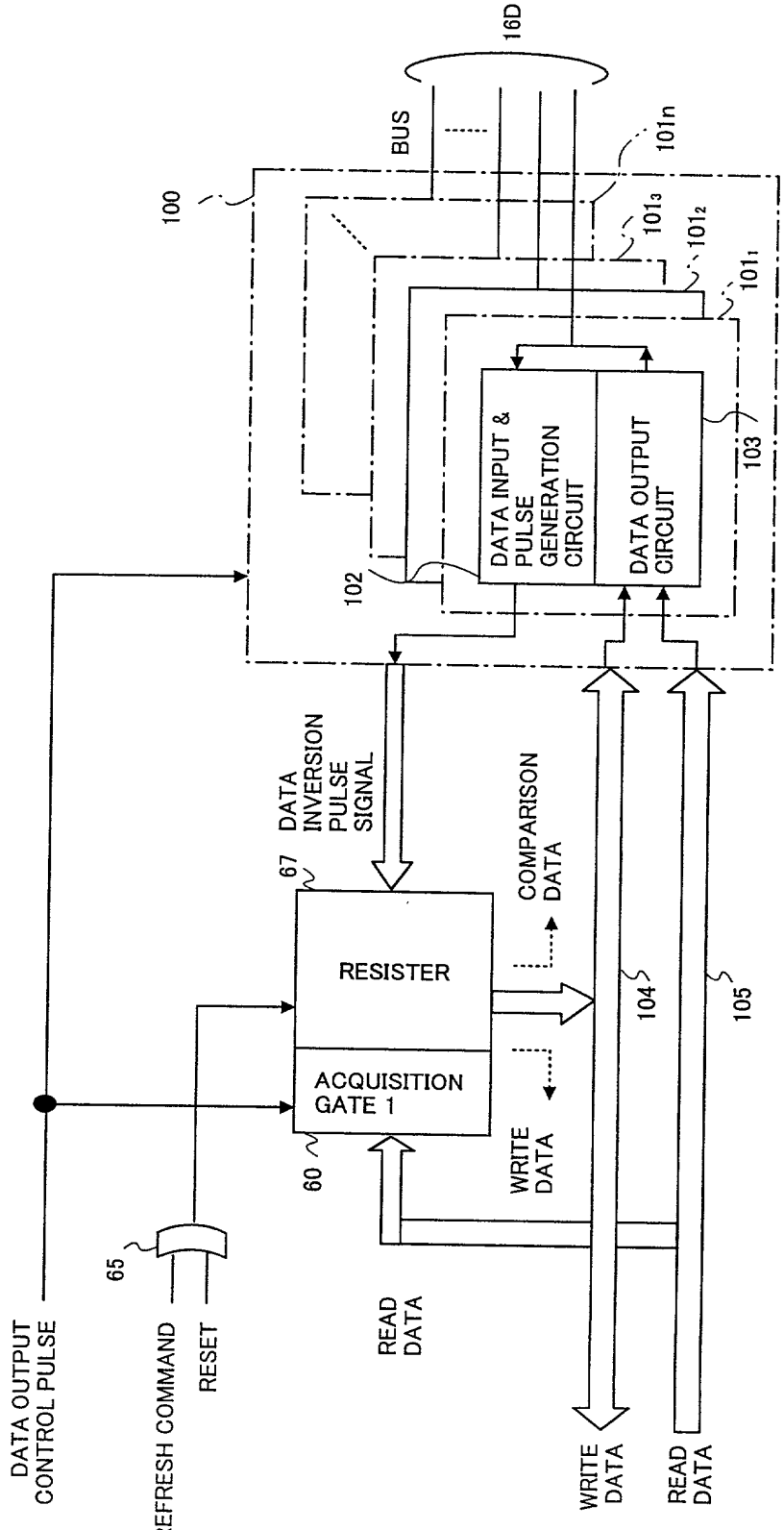

16D
BUS
100
101n
101₃
101₂
101₁
DATA INPUT & PULSE GENERATION CIRCUIT
DATA OUTPUT CIRCUIT
103
102
DATA INVERSION PULSE SIGNAL
67
COMPARISON DATA
RESISTER
ACQUISITION GATE 1
60
WRITE DATA
104
105
READ DATA
65
DATA OUTPUT CONTROL PULSE
REFRESH COMMAND
RESET
READ DATA
WRITE DATA

FIG.21

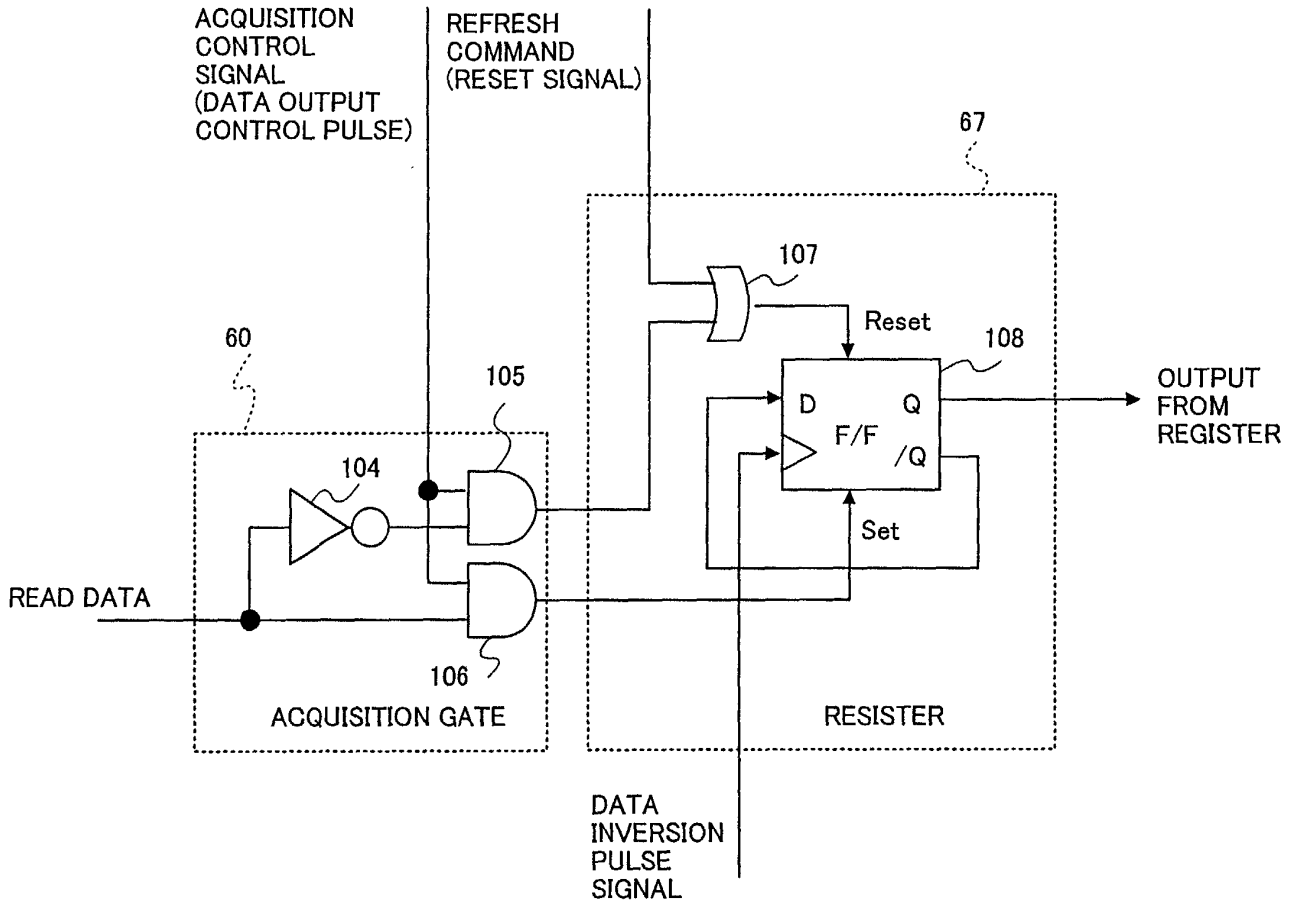


FIG.22

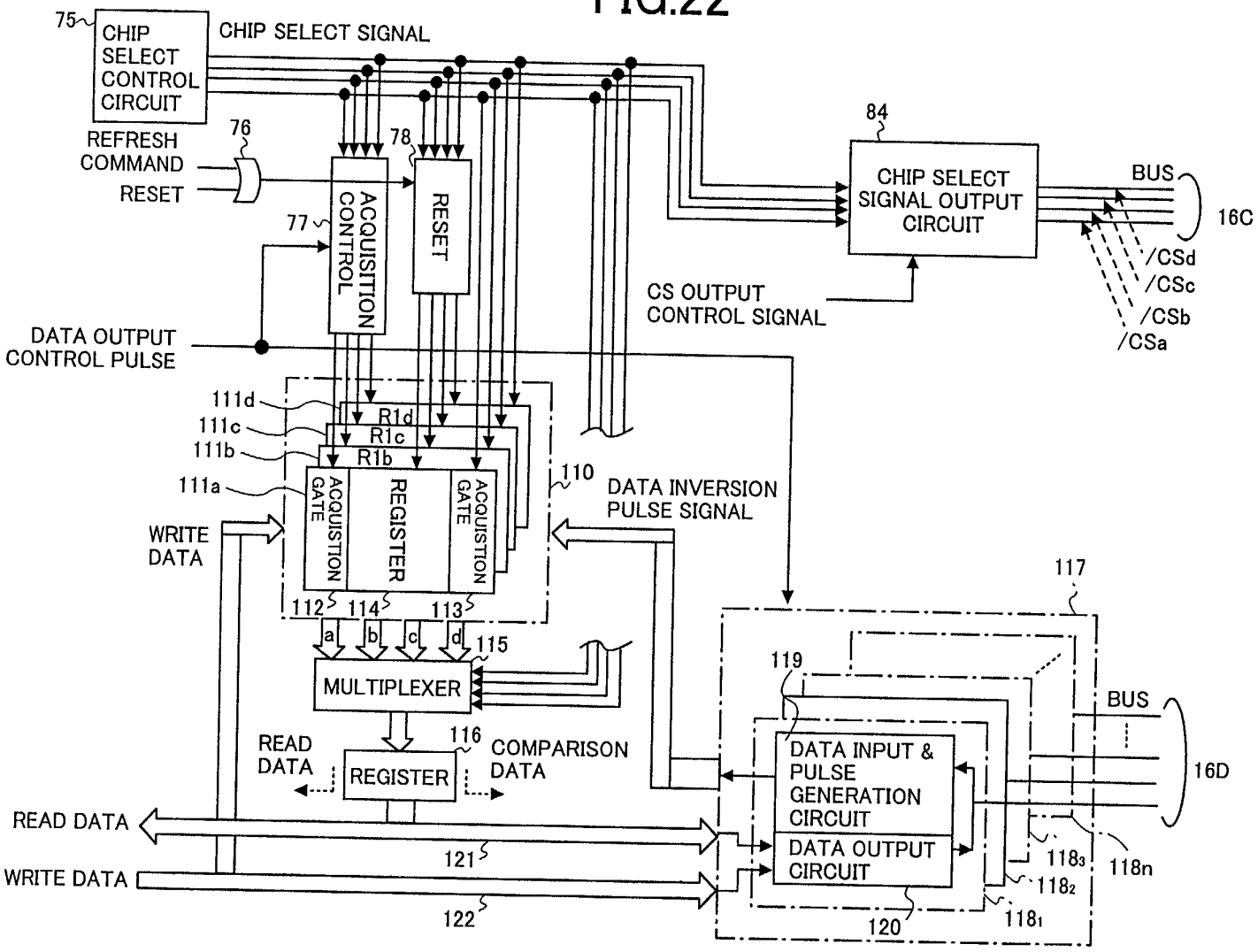


FIG.23

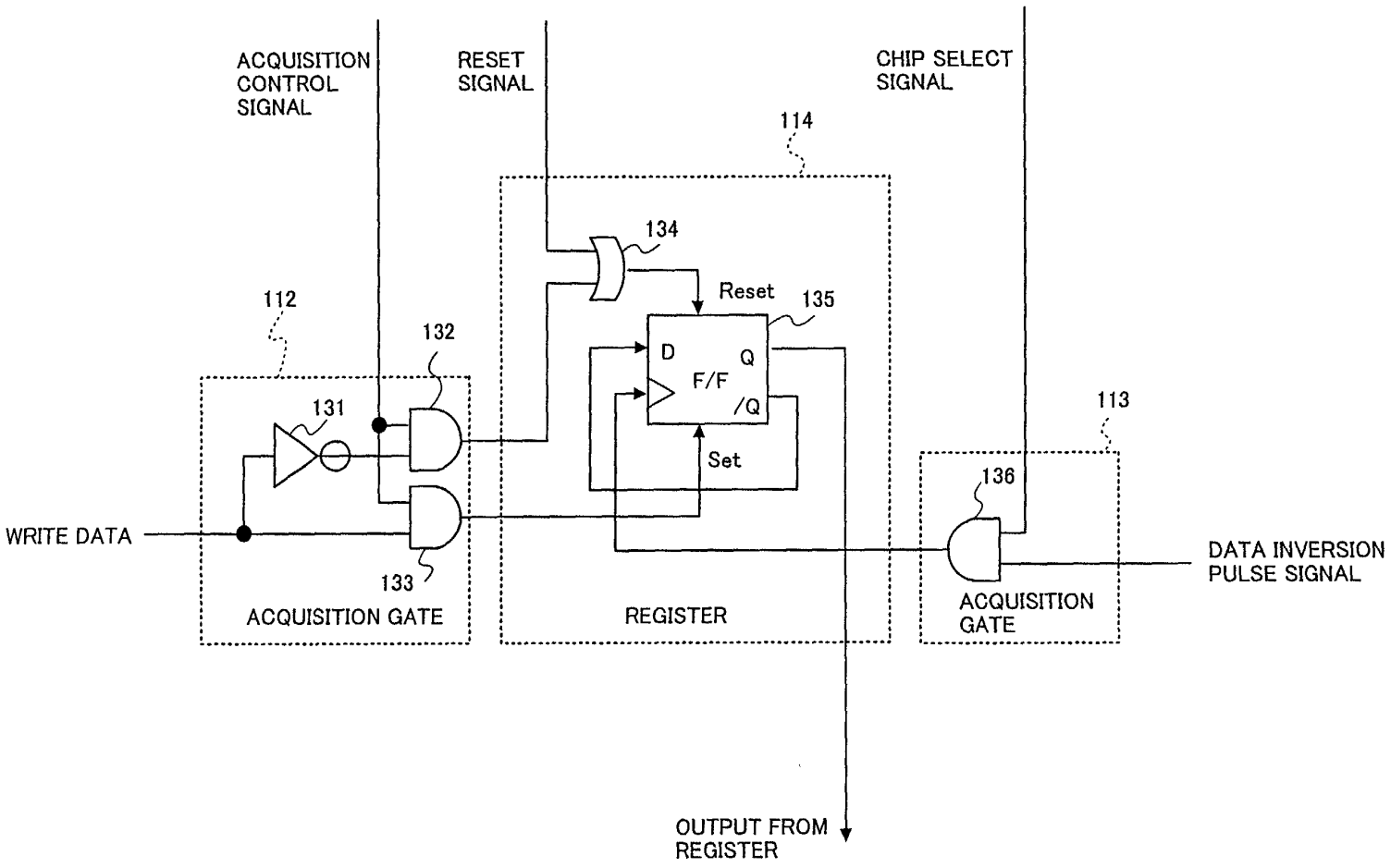


FIG.24A

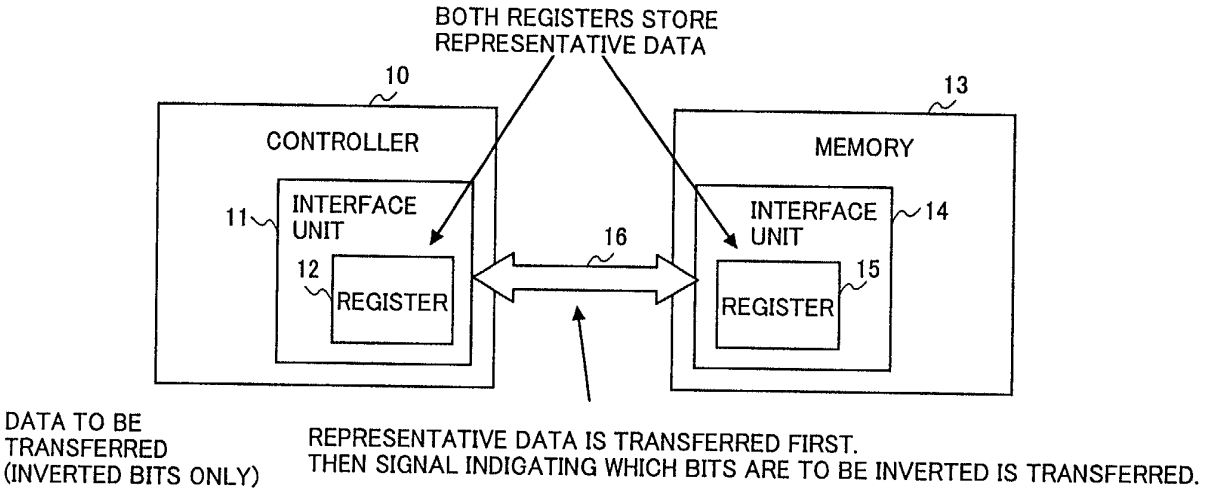


FIG.24B

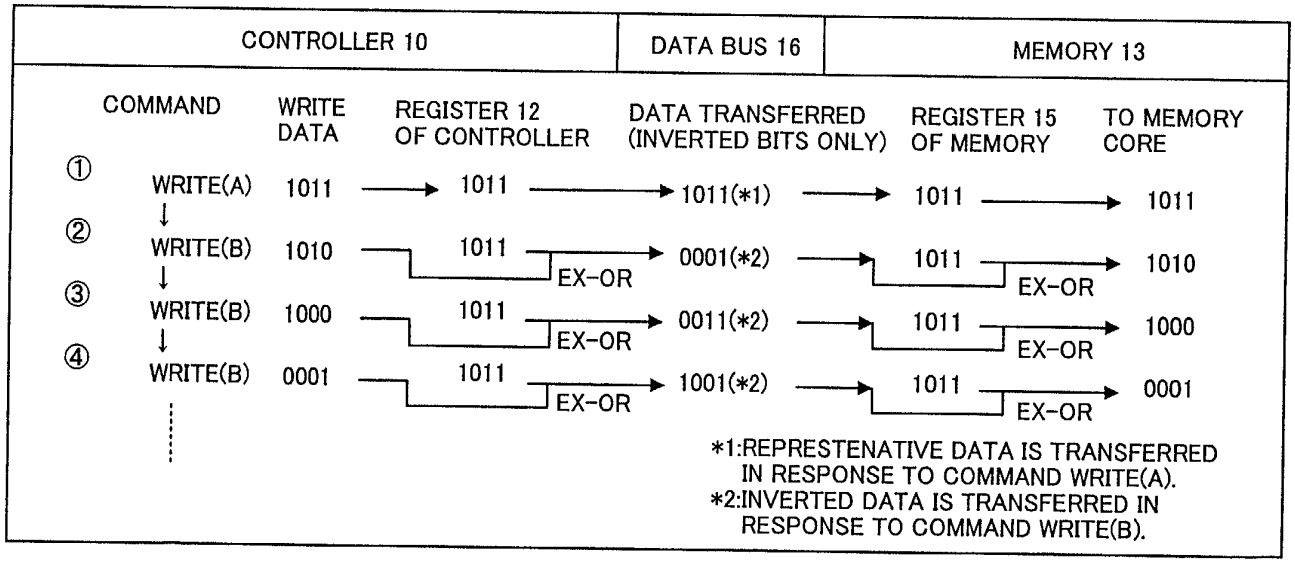


FIG.25

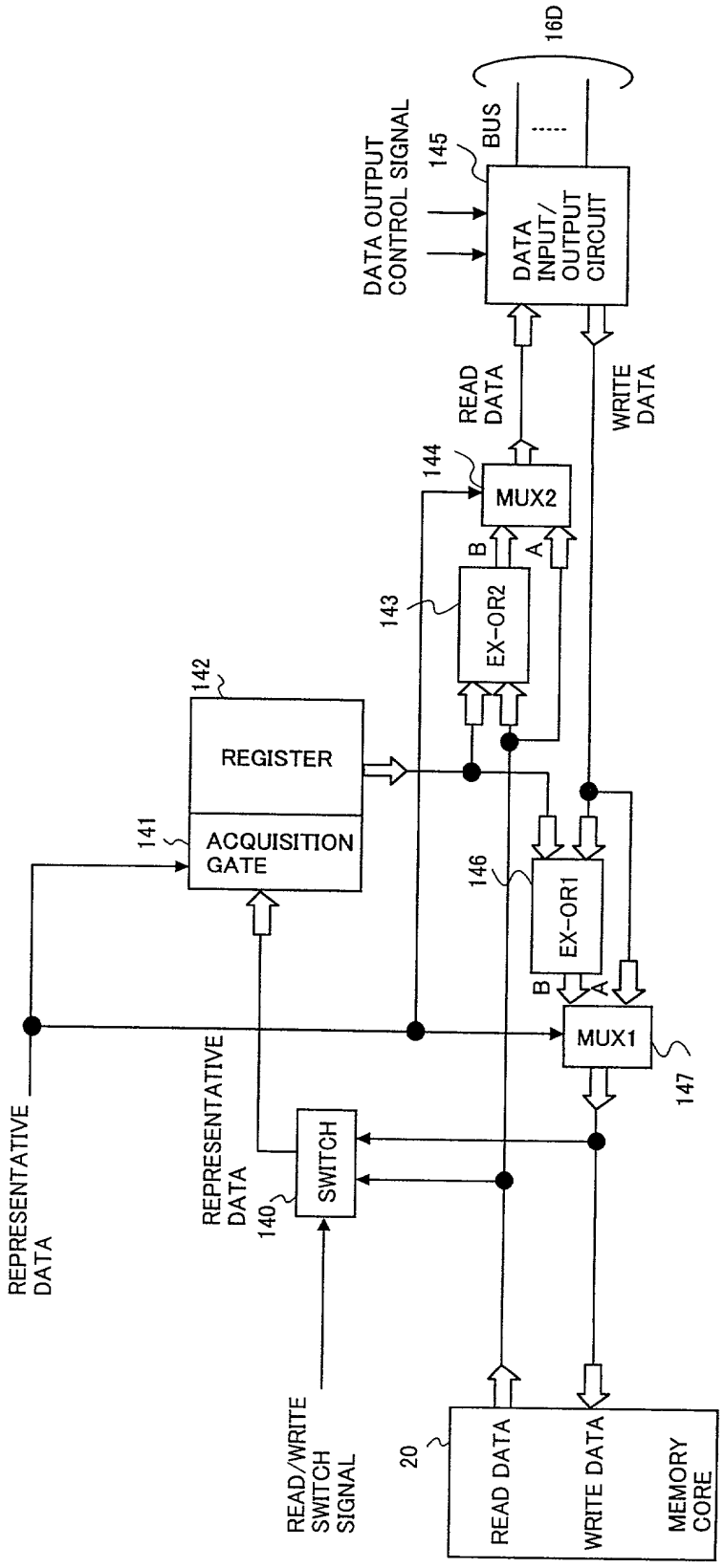

16D
BUS
145
DATA OUTPUT CONTROL SIGNAL
DATA INPUT/ OUTPUT CIRCUIT
READ DATA
WRITE DATA
144
MUX2
B
A
143
EX-OR2
142
REGISTER
141
ACQUISITION GATE
146
EX-OR1
B
A
MUX1
147
REPRESENTATIVE DATA
REPRESENTATIVE DATA
140
SWITCH
READ/WRITE SWITCH SIGNAL
20
READ DATA
WRITE DATA
MEMORY CORE

FIG.26

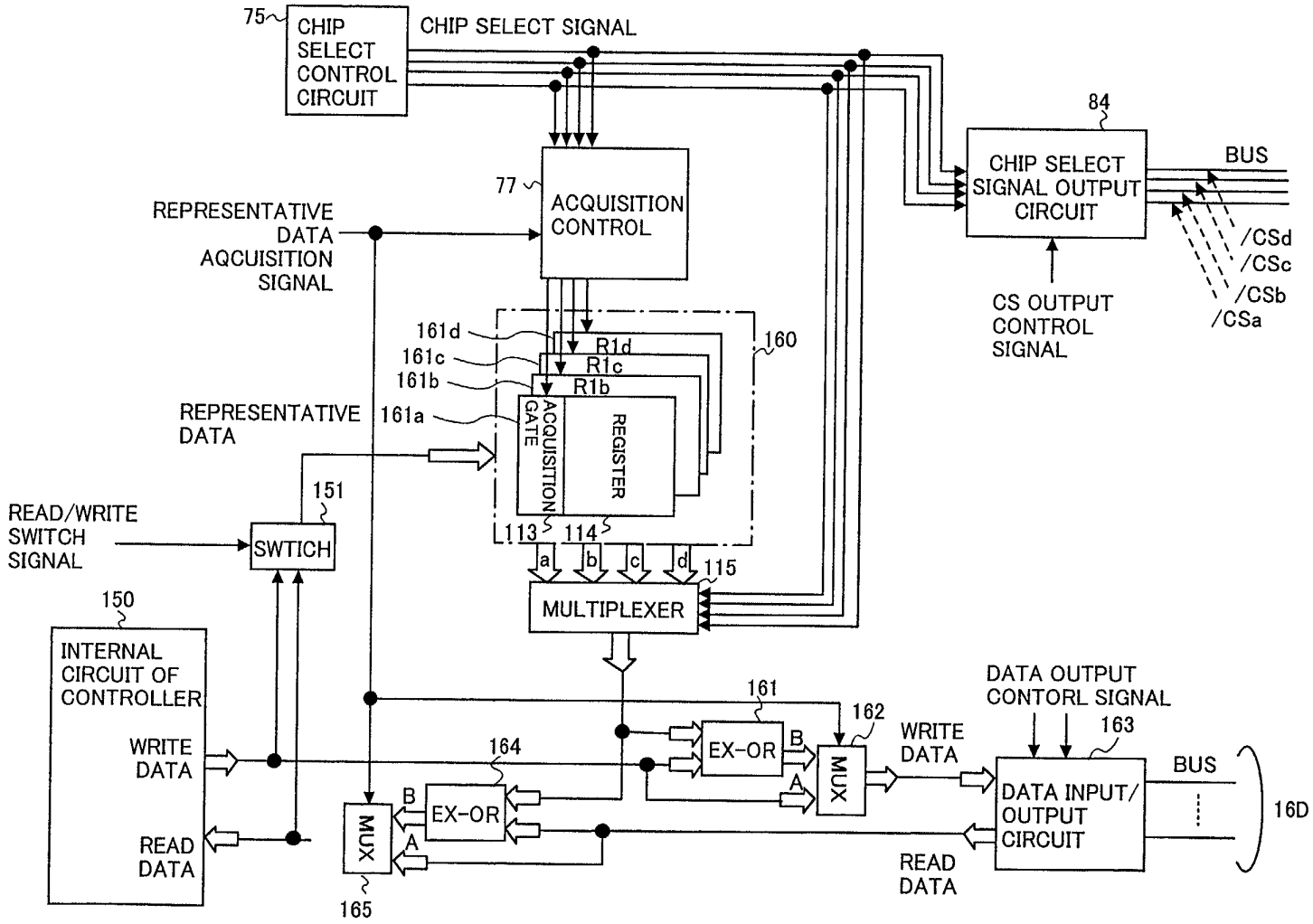
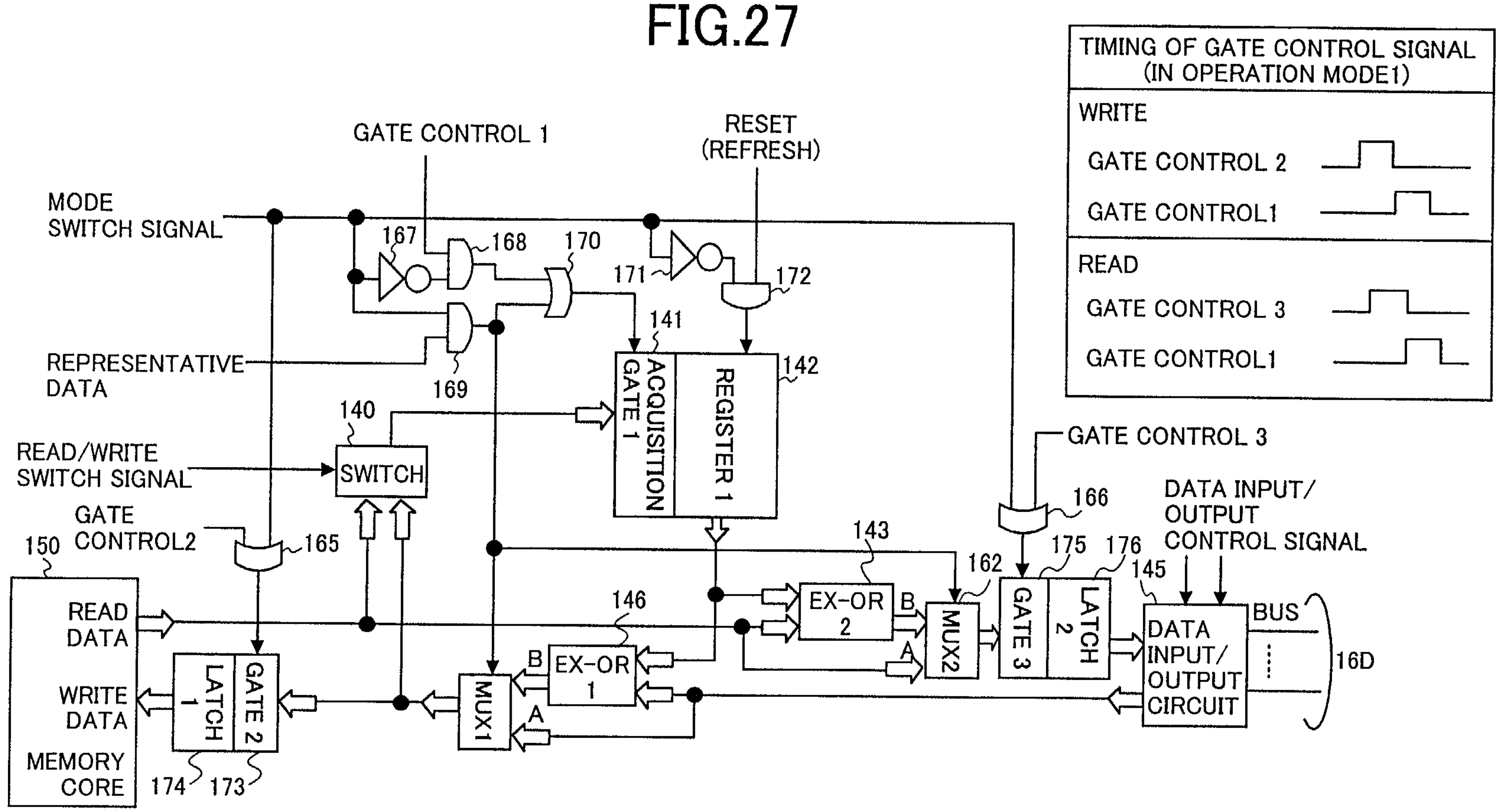

75
CHIP SELECT CONTROL CIRCUIT
CHIP SELECT SIGNAL
84
CHIP SELECT SIGNAL OUTPUT CIRCUIT
BUS
/CSd
/CSc
/CSb
/CSa
CS OUTPUT CONTROL SIGNAL
77
ACQUISITION CONTROL
REPRESENTATIVE DATA AQCUISITION SIGNAL
161d
161c
161b
161a
R1d
R1c
R1b
160
ACQUISITION GATE
REGISTER
REPRESENTATIVE DATA
151
READ/WRITE SWITCH SIGNAL
SWTICH
113
114
a
b
c
d
115
MULTIPLEXER
150
INTERNAL CIRCUIT OF CONTROLLER
WRITE DATA
READ DATA
161
162
164
EX-OR
B
A
MUX
WRITE DATA
DATA OUTPUT CONTORL SIGNAL
163
DATA INPUT/ OUTPUT CIRCUIT
BUS
16D
READ DATA
165

FIG.27



OPERATION MODE 1
(CORRESPONDING TO FIRST PRINCIPLE)

MODE SWITCH SIGNAL=LOW
ACQUISTION GATE 1: CONTROLLED BY GATE CONTROL 1 SIGNAL
MUX1,MUX2:INPUT B IS SELECTED(FIXED)
GATE 2: CONTROLLED BY GATA CONTROL 2 SIGNAL
GATE 3: CONTROLLED BY GETA CONTROL 3 SIGNAL
REGISTER 1 IS RESET IN RESPONSE TO REFRESH

OPERATION MODE 2
(CORRESPONDING TO SECOND PRINCIPLE)

MODE SWITCH SIGNAL = HIGH
ACQUISITION GATE 1, MUX1, MUX2: CONTROLLED BY REPRESENTATIVE DATA ACQUISITION SIGNAL
GATE 2, GATE 3: OPEN (FIXED)
REGISTER 1 IS NOT RESET IN RESPONSE TO REFRESH